APS search

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     (FILE 'USPAT' ENTERED AT 09:40:40 ON 19 JAN 1999)
L1           154 S 711/213/CCLS
L2           739 S LINEAR ADDRESS##
L3          3983 S PHYSICAL ADDRESS##
L4          2265 S VIRTUAL ADDRESS##
L5           238 S CANCEL? (3A) ACCESS?
L6            72 S (SPECULATIVE OR TENTATIVE) (2A) ADDRESS##
L7           113 S L2 AND L3 AND L4
L8             2 S L1 AND L7
L9             4 S L6 AND L1
L10          595 S (PREDICT? OR (LOOK-AHEAD))   (2A) ADDRESS##
L11          637 S L6 OR L10
L12           35 S L11 AND L1
L13            2 S L5 AND L12

=> s l2 and l3 and l4 and l11

L14           16 L2 AND L3 AND L4 AND L11

=> d 1-
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1. 5,860,154, Jan. 12, 1999, Method and apparatus for calculating effective memory addresses; Jeffrey M. Abramson, et al., 711/220; 395/393 [IMAGE AVAILABLE]

2. 5,819,079, Oct. 6, 1998, Instruction fetch on demand for uncacheable memory which avoids memory mapped I/O side effects in a processor with speculative instruction fetch; Andrew F. Glew, et al., 395/584, 586, 800.23; 711/139, 207, 213 [IMAGE AVAILABLE]

3. 5,781,753, Jul. 14, 1998, Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions; Harold L. McFarland, et al., 395/394, 385, 391 [IMAGE AVAILABLE]

4. 5,768,575, Jun. 16, 1998, Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions; Harold L. McFarland, et al., 395/569, 385, 394 [IMAGE AVAILABLE]

5. 5,761,691, Jun. 2, 1998, Linearly addressable microprocessor cache; David B. Witt, 711/3 [IMAGE AVAILABLE]

6. 5,751,981, May 12, 1998, High performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format; David B. Witt, et al., 395/380, 376, 386, 387, 391, 394; 711/201 [IMAGE AVAILABLE]

7. 5,721,855, Feb. 24, 1998, Method for pipeline processing of instructions by controlling access to a reorder buffer using a register file outside the reorder buffer; Glenn J. Hinton, et al., 395/394, 393

[IMAGE AVAILABLE]

8. 5,694,568, Dec. 2, 1997, Prefetch system applicable to complex memory access schemes; Williams Ludwell Harrison, III, et al., 711/213, 137, 220, 221 [IMAGE AVAILABLE]

9. 5,664,136, Sep. 2, 1997, High performance superscalar microprocessor including a dual-pathway circuit for converting cisc instructions to risc operations; David B. Witt, et al., 395/384, 376, 388, 391 [IMAGE AVAILABLE]

10. 5,655,098, Aug. 5, 1997, High performance superscalar microprocessor including a circuit for byte-aligning cisc instructions stored in a variable byte-length format; David B. Witt, et al., 395/386, 376, 380, 389, 586; 711/201 [IMAGE AVAILABLE]

11. 5,655,097, Aug. 5, 1997, High performance superscalar microprocessor including an instruction cache circuit for byte-aligning CISC instructions stored in a variable byte-length format; David B. Witt, et al., 395/380, 376, 382, 386; 711/147 [IMAGE AVAILABLE]

12. 5,651,125, Jul. 22, 1997, High performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating point operations; David B. Witt, et al., 395/394, 306, 391, 393; 711/146 [IMAGE AVAILABLE]

13. 5,623,619, Apr. 22, 1997, Linearly addressable microprocessor cache; David B. Witt, 711/3; 364/243.41, 256.5, DIG.1; 395/800.23; 711/202 [IMAGE AVAILABLE]

14. 5,623,614, Apr. 22, 1997, Branch prediction cache with multiple entries for returns having multiple callers; Korbin S. Van Dyke, et al., 395/587; 364/DIG.1 [IMAGE AVAILABLE]

15. 5,287,487, Feb. 15, 1994, Predictive caching method and apparatus for generating a **predicted address** for a frame buffer; Curtis Priem, et al., 711/204; 364/256.8, 263.1, 939.7, 948, 955, DIG.1, DIG.2 [IMAGE AVAILABLE]

16. 5,265,213, Nov. 23, 1993, Pipeline system for executing predicted branch target instruction in a cycle concurrently with the execution of branch instruction; Uri C. Weiser, et al., 395/587; 364/229.2, 231.8, 232.23, 238, 239, 243, 243.4, 243.41, 243.42, 244, 244.3, 255.1, 259, 259.2, 259.9, 261.3, 261.5, 261.7, 262.4, 262.9, 263.1, 271.9, 281.3, 281.4, DIG.1; 395/383 [IMAGE AVAILABLE]